"Express Mail" mailing label number EL392680044US
Date of Deposit: December 1, 2000

Case No. 9076/468
AMD Docket No. E370

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Shields et al.	)
Serial No. To Be Assigned	)
Filing Date: Herewith	) Examiner: To Be Assigned
For A DUAL SPACER PROCESS FOR NON-VOLATILE MEMORY DEVICES	) Group Art Unit No.: To Be Assigned

PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, D.C. 20231
Dear Sir:

This is a regular application claiming priority under 35 U.S.C. § 119 (e) of the United States provisional application serial number 60/190,475. Prior to examination on the merits, please enter the amendment below.

In the Specification:

Please amend the specification as follows:

Please insert the following paragraph immediately before the first line:

--CROSS-REFERENCE TO RELATED APPLICATION

This application claims the benefit under 35 U.S.C. § 119(e) of the United States provisional application serial no. 60/190,475, filed on March 17, 2000.--

Page 5, line 26, delete "oxide deposition" and in its place insert --first oxide layer 12--;

line 28, delete "deposition" and in its place insert --layer--;

line 29, delete "first oxide"; and after "deposition" insert --of first oxide layer--;

line 30, delete "are" and it its place insert --is--.

Page 6, line 1, delete "spacer" and it its place insert --the--; and after "formation" insert

of spacer 12'--;

line 4, delete "deposited" and in its place insert --formed--; and after "the" (second occurrence) insert --formation of--;

line 5, delete "13 deposition" and in its place insert --13'--;

line 13, delete "deposition";

line 19, delete "the oxide deposition" and in its place insert --the deposition of first oxide layer--; and delete "reduce" and in its place insert --reduced--;

line 21, after "the" insert --first--;

line 23, delete "a second spacer deposition 13" and in its place insert --the deposition of a second oxide layer 13";

line 24, delete "second spacer"; and after "deposition" insert --of second oxide layer--;

line 26, delete "spacer deposition" and in its place insert --oxide layer--;

line 27, delete "spacer deposition" and in its place insert --oxide layer--;

line 30, delete "second";

line 31, after "deposition" insert --of the second oxide layer--; and delete "of the spacer oxide".

Page 7, line 2, after "area" insert --20--;

line 3, delete "20" and insert --4--;

line 8, after "core" insert --24--;

line 21, after "the" (first occurrence) insert --deposition of the--; delete "deposition" and in its place insert --layers 12, 13--; and delete "preformed" and in its place insert --performed--;

line 29, after "the" (first occurrence) insert --deposition of the--; delete "deposition" and insert --layers 12, 13--; and delete "preformed" and in its place insert --performed--.

Page 8, line 7, delete "spacer" and in its place insert --oxide--.

In the Claims:

Please amend the claims as follows:

1. (Amended) A method for forming a spacer, comprising:

depositing [an] a first oxide layer over [a] at least two polysilicon [line] lines of a core and periphery area;

performing a first spacer etch in the core and periphery area;

implanting an area located between two polysilicon lines in the core area;

applying a second oxide layer over the core and periphery areas; and

performing a second spacer etch over the periphery area wherein a [difference] different appearance of the core and periphery area is produced.

2. The method of claim 1 wherein the first oxide [deposition] layer has a thickness of less than one-half the distance between a periphery of [the] adjacent polysilicon lines.

3. A [non volatile] non-volatile memory device made by the method of claim 1.

4. A [non volatile] non-volatile memory device made by the method of claim 2.

Please add the following new claims:

5. A process for fabricating a non-volatile memory device comprising:

providing a substrate having a core area, a periphery area, and at least two polysilicon lines overlying the core area and the periphery area;

depositing a first oxide layer over the polysilicon lines;

performing a first spacer etch in the core area and the periphery area;

implanting an area located between at least two polysilicon lines in the core area;

depositing a second oxide layer over the core and periphery areas; and

performing a second spacer etch over the periphery area.

6. The process of claim 5, wherein the first oxide layer has a thickness of less than one-half the distance between a periphery of adjacent polysilicon lines.

7. The process of claim 5 further comprising performing a second spacer etch over the core area.

8. The process of claim 5, wherein the implanting of an area occurs after the performing of the first spacer etch.

9. The process of claim 5, further comprising implanting an area located between at least two polysilicon lines in the periphery area.

10. The process of claim 9, wherein the implanting of an area located between at least two polysilicon lines in the periphery area occurs after the performing of the first spacer etch.

11. The process of claim 9, wherein the implanting of an area located between at least two polysilicon lines in the core area occurs after the performing of the second spacer etch.

12. A process for making an electronic component comprising:
forming a memory cell by the process of claim 5; and
forming the electronic component comprising the memory cell.

13. A process for fabricating a memory cell comprising the steps of:
providing a substrate having a core area, a periphery area, at least two polysilicon lines overlying the core area and the periphery area, and first spacers adjacent the at least two polysilicon lines overlying the core area and the periphery area; and

forming a second spacer adjacent at least one first spacer.

14. The process of claim 13, further comprising implanting an area located between at least two polysilicon lines in the core area.

REMARKS

With this Amendment, the application is in condition for early action on the merits. Should the Examiner deem a telephone conference to be helpful in expediting allowance of this application, the Examiner is invited to call the undersigned at the telephone number shown below.

Respectfully submitted,

David Rozenblat
Registration No. 47,044
Attorney for Applicant

BRINKS HOFER GILSON & LIONE
P.O. BOX 10395
CHICAGO, ILLINOIS 60610
(312) 321-4200